Please type a plus sign (+) inside this box [+]

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P5549 Total Pages 5

First Named Inventor or Application Identifier Zohar Bogin, et al.

Express Mail Label No. EL034160545US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 29)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 8)

4. X Oath or Declaration (Total Pages 5) (UNSIGNED)

a. ___ Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. ___ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ___ Computer Readable Copy
b. ___ Paper Copy (identical to computer copy)
c. ___ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)

_____ b. Power of Attorney

10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449

_____ b. Copies of IDS Citations

12. _____ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)

b. Statement filed in prior application, Status still proper and desired

15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. X Other: Copy of Postcard with Express Mail Label

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

____ Continuation ____ Divisional ____ Continuation-in-part (CIP)

of prior application No: _____

18. **Correspondence Address**

_____ Customer Number or Bar Code Label _____ (Insert Customer No. or Attach Bar Code Label here)

or

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PTO/SB/17(10/96)
Approved for use through 09/30/98. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL

TOTAL AMOUNT OF PAYMENT ($) 1144.00

Complete if Known:
Application No. Unassigned
Filing Date December 4, 1998
First Named Inventor Zohar Bogin, et al.
Group Art Unit Unassigned
Examiner Name Unassigned
Attorney Docket No. 042390.P5549

METHOD OF PAYMENT (check one)

1. [X] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

Deposit Account Number 02-2666
Deposit Account Name

[X] **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17**

[ ] **Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance, 37 CFR 1.131(b)**

2. X **Payment Enclosed**
X **Check**
____ **Money Order**
____ **Other**

FEE CALCULATION (fees effective 10/01/97)

1. **FILING FEE**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	760	201	380	Utility application filing fee	760.00
106	310	206	155	Design application filing fee	
107	480	207	240	Plant filing fee	
108	760	208	380	Reissue filing fee	
114	150	214	75	Provisional application filing fee	

SUBTOTAL (1) $ 760.00

2. **CLAIMS**

			Extra		Fee from below		Fee Paid
Total Claims	37	- 20 =	17	X	18	=	$306.00
Independent Claims	4	- 3 =	1	X	78	=	$ 78.00
Multiple Dependent Claims				X		=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
103	18	203	9	Claims in excess of twenty	306.00
102	78	202	39	Independent claims in excess of 3	78.00
104	260	204	130	Multiple dependent claim	
109	78	209	39	Reissue independent claims over original patent	
110	18	210	9	Reissue claims in excess of 20 and over original patent	

SUBTOTAL (2) $ 384.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	380	216	190	Extension for response within second month	
117	870	217	435	Extension for response within third month	
118	1,360	218	680	Extension for response within fourth month	
128	1,850	228	925	Extension for response within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,210	241	605	Petition to revive unintentionally abandoned application	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	760	246	380	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	760	249	380	For each additional invention to be examined (see 37 CFR 1.129(a))	
				Other fee (specify) _____	
				Other fee (specify) _____	

SUBTOTAL (3)$ 0

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: Darren J. Milliken

Signature _____ Date 12/4/98

Reg. Number 42,004 Deposit Account User ID _____ (complete if applicable)

PTO/SB/17 (10-96)
Approved for use through 09/30/98 OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT APPLICATION

for

METHOD AND APPARATUS FOR SELF TIMING REFRESH

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"Express Mail" mailing label number EL034160545US

Date of Deposit December 4, 1998

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Beatrice Orozco
(Typed or printed name of person mailing paper or fee)

Beatrice Orozco
(Signature of person mailing paper or fee)

METHOD AND APPARATUS FOR SELF TIMING REFRESH

FIELD OF THE INVENTION

The present invention relates to memory systems; more particularly, the present invention relates to triggering refreshes in a memory system.

BACKGROUND OF THE INVENTION

Mobile computer systems are capable of shutting down power to most of its subsystems while maintaining the content of the memory. This provides a mobile computer with a low power mode that enables power conservation. The low power mode may be entered following a period of inactivity while the computer is powered up. From the low power mode, the mobile computer can quickly resume complete system operation. While operating in the low power mode, the main memory must be periodically refreshed to recharge electrical cells in order to maintain data integrity. Accordingly, a system memory controller within the computer system typically refreshes the main memory while the computer is operating in the low power mode.

Figure 1 is a block diagram of an exemplary computer system 100. Computer system 100 includes processor 105 coupled to processor bus 110. Processor 105 is also coupled to memory controller 120. Main memory 113 is coupled to processor

bus 110 through memory controller 120. Main memory 113 stores sequences of instructions that are executed by processor 105. Processor bus 110 is also coupled to a Peripheral Component Interconnect (PCI) standard bus 130 by memory controller 120. Bus bridge 140 couples PCI bus 130 to an Industry Standard Architecture (ISA) bus 150.

Memory controller 120 is also coupled to bus bridge 140 via a power status line (STAT) and an external clock source (PDRCLK). A STAT signal is transmitted from bus bridge 140 to memory controller 120 in order to indicate whether computer system 100 is in the low power mode. PDRCLK provides a clock source to memory controller 120 during the low power mode in order to provide a reference for triggering main memory refreshes.

One problem with typical computer systems such as computer system 100 is that providing an external clock source, such as PDRCLK, to trigger a memory refresh requires an additional pin to be used at memory controller 120. The presence of additional pins at memory controller 120 may potentially lead to an increase in circuit complexity within computer system 100. Further, additional pins may result in an increase in the cost of manufacturing memory controller 120. Therefore, it would be desirable to provide a memory controller with an internal clock source for triggering a memory refresh.

SUMMARY OF THE INVENTION

According to one embodiment, the present invention discloses a computer system that includes a memory and a memory controller. The memory controller includes a refresh timing circuit that generates clock pulses. The clock pulses are used to trigger memory refresh events.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the invention. The drawings, however, should not be taken to limit the invention to the specific embodiments, but are for explanation and understanding only.

Figure 1 is a block diagram of an exemplary embodiment of a computer system.

Figure 2 is a block diagram of one embodiment of a computer system in accordance with one embodiment of the present invention.

Figure 3 is a memory controller in accordance with one embodiment of the present invention.

Figure 4 is a block diagram of refresh timing unit in accordance with one embodiment of the present invention.

Figure 5 is a flow diagram of the operation of a refresh timing unit in accordance with one embodiment of the present invention.

Figure 6 is a flow diagram of the operation of a refresh timing unit in accordance with one embodiment of the present invention.

Figure 7 is a block diagram of refresh timing unit in accordance with one embodiment of the present invention; and

Figure 8 is a block diagram of an internal clock generator in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

Figure 2 is a block diagram of one embodiment of a computer system 200. Computer system 200 includes processor 205 coupled to processor bus 210. In one embodiment, processor 205 is a processor in the Pentium® family of processors including the Pentium® II family and mobile Pentium® and Pentium® II processors available from Intel Corporation of Santa Clara, California. Alternatively, other processors may be used. Processor 205 may include a first level (L1) cache memory (not shown in Figure 1).

In one embodiment, processor 205 is also coupled to cache memory 207, which is a second level (L2) cache memory, via dedicated cache bus 202. The L1 and L2 cache memories can also be integrated into a single device. Alternatively, cache memory 207 may be coupled to processor 205 by a shared bus. Cache memory 207 is optional and is not required for computer system 200.

Chip set 220 is also coupled to processor bus 210. In one embodiment, chip set 220 is the 440BX chip set available from Intel Corporation; however, other chip sets can also be used. Chip set 220 may include a memory controller for controlling a main memory 213. Main memory 213 is coupled to processor bus 210 through chip set 220. Main memory 213 and cache memory 207 store sequences of instructions that are executed by processor 205. In one embodiment, main memory 213 includes

an extended data out dynamic random access memory (EDO DRAM); however, main memory 213 may have other configurations. The sequences of instructions executed by processor 205 may be retrieved from main memory 213, cache memory 207, or any other storage device. Additional devices may also be coupled to processor bus 210, such as multiple processors and/or multiple main memory devices. Computer system 200 is described in terms of a single processor; however, multiple processors can be coupled to processor bus 210. Video device 225 is also coupled to chip set 220. In one embodiment, video device includes a video monitor such as a cathode ray tube (CRT) or liquid crystal display (LCD) and necessary support circuitry.

Processor bus 210 is coupled to system bus 230 by chip set 225. In one embodiment, system bus 230 is a Peripheral Component Interconnect (PCI) standard bus; however, other bus standards may also be used. Multiple devices, such as audio device 227, may be coupled to system bus 230.

Bus bridge 240 couples system bus 230 to secondary bus 250. In one embodiment, secondary bus 250 is an Industry Standard Architecture (ISA) bus; however, other bus standards may also be used, for example Extended Industry Standard Architecture (EISA). Multiple devices, such as hard disk 253 and disk drive 254 may be coupled to secondary bus 250. Other devices, such as cursor control devices (not shown in Figure 2), may be coupled to secondary bus 250.

According to one embodiment, computer 200 operates in either a normal mode or a low power mode. Computer system 200 is in the low power mode whenever power is shutdown to most of its subsystems (e.g., processor 205, and video device 225). However, the content of main memory 213 is maintained while computer system 200 is in the low power mode.

Figure 3 illustrates a memory controller 300 in accordance with one embodiment of the present invention. Memory controller 300 includes memory interface control unit 310, refresh unit 320 and refresh timing unit 330. Memory controller 300 accesses main memory 213 based upon commands received from processor 205 and one or more peripheral devices such as video device 227 coupled to chip set 220. Memory controller 300 may read data from, and write data to, main memory 213. For some operations such as main memory refresh, memory controller 300 must access all portions of main memory 213 within a deterministic time period. According to one embodiment, memory controller 300 is included within chip set 220.

Memory interface control unit 310 is coupled to refresh unit 320 and refresh timing unit 330. Memory interface control unit 310 coordinates access to main memory 213 by various agents, such as processor 205, video device 225 and refresh unit 320. In addition, memory interface control unit 310 transmits memory cycles to

main memory 113. One of ordinary skill in the art will appreciate that other agents or devices may be coupled to memory interface control unit 310 in order to gain access to main memory 213.

Refresh unit 320 is coupled to refresh timing unit 330 and recharges electrical cells within main memory 213 in order to maintain data integrity. Refresh unit receives a REFRESH signal from refresh timing unit 330 in order to trigger a refresh event. Refresh unit 320 also receives a power status signal (STAT) from bus bridge 240. STAT is an indicator of whether computer system 200 is operating in a normal mode or a low power mode. The low power mode of operation enables power conservation whenever computer system 200 is powered up, but has not recently been used. Additionally, refresh unit 230 receives HOST CLK from processor 205.

Refresh timing unit 330 also receives the HOST CLK and STAT signals. In addition, refresh timing unit 330 receives a reset signal (RST) that is used to reset circuitry internal to refresh timing unit 330. **Figure 4** is a block diagram of refresh timing unit 330 in accordance with one embodiment of the present invention. Refresh timing unit 330 includes an internal clock generator 432, counter 434, buffer 436, comparator 438 and multiplexer 450.

Refresh timing unit 330 triggers main memory 213 refresh events. Refresh events are triggered based upon HOST CLK whenever computer system 200 is

operating in the normal mode. HOST CLK is a timing reference used to generate normal refreshes at repeatable deterministic intervals. According to one embodiment, memory refreshes are triggered every 15.6 microseconds. However, one of ordinary skill in the art will appreciate that refresh cycles may occur at other frequencies. Refresh timing unit 330 also triggers refresh events whenever computer system 200 is operating in the low power mode.

Internal clock generator 432 generates refresh trigger events, both in the normal mode and low power mode. **Figure 8** is a block diagram of internal clock generator 432. Internal clock generator 432 includes a host clock refresh counter 834 and clock generator 836. Host clock refresh counter 834 is a logic block that references the HOST CLK signal in order to generate a refresh trigger (N_REFRESH) whenever computer system 200 is operating in the normal mode. Host clock refresh counter 834 also generates a NORM_RST and LOAD signal. Clock generator 836 generates an oscillating clock signal (OSCLK) that triggers memory refreshes in the low power mode of operation for computer system 200. However, clock generator 836 is active at all times (i.e., in normal mode and low power mode).

According to one embodiment, clock generator 836 is a ring oscillator implemented using a chain of thirty-six (37) serially coupled inverters. The OSCLK signal is generated each time a signal completely propagates through the chain of

inverters. One of ordinary skill in the art will appreciate that clock generator 836 may be implemented using other quantities of inverters. Further, other clock generation methods may be used to implement clock generator 836.

Referring back to **Figure 4**, counter 434 is coupled to internal clock generator 432 and increments each time an OSCLK pulse is received from clock generator 836. Counter 434 counts the number of OSCLK pulses generated while computer system 200 operating in both the normal and low power modes. Counter 434 also receives the STAT, RST and NORM-RST signals. Counter 434 receives the RST signal for initialization upon system startup. The NORM-RST signal is received at counter 434 in order to provide a reset after each refresh in the normal mode. Additionally, an LP_RST signal is received from comparator 438 after each refresh in low power mode in order to reset counter 434.

Further, counter 434 transmits a COUNT signal to comparator 438 after each increment at times computer system 200 is operating in the low power mode. Counter 434 also transmits a VALUE signal to buffer 436. VALUE represents the number of OSCLK pulses received by counter 434 between normal mode memory refreshes. Buffer 436 is coupled to counter 434 and stores the VALUE signals received from counter 434. Buffer 436 accepts the VALUE signals upon receiving

the LOAD signal from host clock refresh counter 834 within internal clock generator 432. LOAD indicates that a normal refresh has been triggered and that new VALUE signals are ready to be transferred to buffer 436.

In addition, buffer 436 transmits a BUF signal to comparator 438 whenever computer system 200 transitions from the normal mode to the low power mode. BUF represents the frequency at which refresh events are to be triggered during low power mode operation. According to one embodiment, buffer 436 is implemented using one or more storage registers. However, one of ordinary skill in the art will appreciate that other memory devices may be used to implement buffer 436.

Comparator 438 is coupled to internal clock generator 432, counter 434, buffer 436 and multiplexer 450. Comparator 438 compares the COUNT signal received from counter 434 with the BUF signal received from buffer 436 while computer system 200 is operating in the low power mode. Once a match is detected between COUNT and BUF, a signal (LP_REFRESH) is transmitted to multiplexer 450. Also, comparator 438 transmits the LP_RST signal to counter 434 upon a match between COUNT and BUF.

Multiplexer 450 selects between the N_REFRESH and LP_REFRESH signals based upon the STAT signal. If STAT indicates that computer system 200 is operating in the normal mode, N_REFRESH is transmitted to refresh unit 320 as

REFRESH in order to trigger a memory refresh. However, if STAT indicates that computer system 200 is operating in the low power mode, LP_REFRESH is transmitted as REFRESH.

As described above, memory refreshes are triggered based upon a HOST CLK reference whenever computer system 200 is operating in the normal mode. After a normal mode refresh, counter 434 is reset upon receiving the NORM_RST signal. **Figure 5** is a flow diagram of the operation of refresh timing unit 330 while operating in the normal mode. At process block 510, counter 434 commences to count OSCLK pulses generated by clock generator 836. Counter 434 increments upon each received OSCLK pulse. OSCLK pulses are counted until a subsequent memory refresh is triggered by host clock counter 834. Alternatively, as will be described later, counter 434 is interrupted upon receiving the STAT signal indicating a transition into the low power mode.

At process block 520, a subsequent memory refresh is triggered by host clock counter 834. As described above, memory refreshes are triggered every 15.6 microseconds. At process block 530, the incremented count (i.e., the number of OSCLK pulses received by counter 434 between normal refresh cycles) is transmitted to buffer 436 as VALUE. At process block 540, counter 434 is again reset after the refresh, and control is returned to process block 510 wherein counter 434 begins

counting OSCLK pulses again. According to one embodiment, the normal mode operation of refresh timing unit 330 is continually repeated in order to periodically update the number of OSCLK pulses that occur during a refresh cycle. Consequently, timing refresh unit continuously tracks of the number of OSCLK pulses that occur between memory refreshes whenever it is operating in the normal mode.

The tracking of OSCLK pulses that occur while computer system 200 is operating in the normal mode is essentially a calibration feature of the present invention. The number of OSCLK transitions that occur between each normal refresh dictates the number of OSCLK pulses that are to be received by counter 434 before triggering a low power mode refresh. However, due to the potential difference of voltage and temperature conditions, or process skew, within computer system 200, operating conditions may vary. Accordingly, the frequency of OSCLK pulses generated by clock generator 836 between normal mode refreshes may vary. Hence, refresh timing unit 330 functions as automatic compensation circuitry that continuously evaluates the time between normal refresh events while computer system 200 is in the normal mode of operation.

Upon receiving the STAT signal indicating that computer system 200 is transitioning from the normal mode to the low power mode, the function of refresh timing unit 330 switches from calibration circuitry to a refresh trigger. **Figure 6** is a

flow diagram of the operation of refresh timing unit 330 while operating in the low power mode. At process block 610, refresh timing unit 330 transitions from the normal mode to the low power mode. At process block 620, buffer 436 transmits BUF to comparator 438. As described above, BUF represents the refresh frequency while operating in the low power mode. At process block 630, comparator 438 transmits the LP_RST which causes counter 434 to reset.

At process block 640, counter 434 begins counting OSCLK pulses received from clock generator 836. As each pulse is received, counter 434 is incremented. Each incremented value is, in turn, transmitted to comparator 438 as COUNT. At process block 650, it is determined whether the COUNT value is equal to the BUF value stored in comparator 438. If it is determined that COUNT is unequal to BUF, control is returned to process block 640 wherein counter receives a subsequent OSCLK pulse. If it is determined that COUNT is equal to BUF, comparator 438 is enabled and transmits the LP_REFRESH signal multiplexer 450. Multiplexer 450, in turn, transmits a REFRESH signal to refresh unit 320. Refresh unit arbitrates and is granted access to main memory 213 wherein a refresh is executed.

At process block 670 it is determined whether the STAT signal has been received, indicating a transition from the low power mode back to the normal mode. If it is determined that the STAT signal has not been received, control is returned

back to process block 630 wherein comparator 438 transmits the LP_RST signal and counter 434 is reset. If the STAT signal has been received, refresh timing unit 330 returns to the normal mode of operation, process block 680.

Figure 7 is a block diagram of another embodiment of refresh timing unit 330 in which the functions of counter 434 is divided between counters 733 and 735. In this embodiment, counter 735 operates while computer system 200 is in the normal mode and counter 733 operates while computer system 200 is in the low power mode. Counter 735 is coupled to internal clock generator 432 and buffer 436, and counts OSCLK pulses generated by clock generator 836 between normal mode memory refreshes. Additionally, counter 735 transmits VALUE upon buffer 436 receipt of the LOAD signal indicating a refresh event.

Upon receiving the STAT signal indicating a transition to the low power mode, counter 735 is deactivated and counter 733 is activated. Subsequently, counter 733 begins counting OSCLK pulses and transmitting the incremented COUNT values to comparator 438. Upon a transition from the low power mode back to the normal mode, counter 733 is deactivated and counter 735 is again activated.

Thus, a method and apparatus providing a memory controller with an internal clock source for triggering a memory refresh has been described

CLAIMS

What is claimed is:

1. A computer system comprising:

a memory; and

a memory controller, wherein the memory controller includes a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

2. The computer system of claim 1, wherein the refresh timing circuit triggers memory refresh events whenever the computer system is operating in a normal mode and a low power mode.

3. The computer system of claim 2, wherein the refresh timing circuit further comprises:

a clock generator for generating the clock pulses;

a first counter coupled to the clock generator;

a storage register coupled to the clock generator and the counter; and

a comparator coupled to the clock generator, the counter and the storage register.

4. The computer system of claim 3, wherein the first counter counts the number of clock pulses generated by the clock generator.

5. The computer system of claim 4, wherein the first counter transmits data to the storage register whenever the computer system is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a prior memory refresh event.

6. The computer system of claim 5, wherein the storage register transmits the data to the comparator upon a transition from the normal mode to the low power mode.

7. The computer system of claim 6, wherein the first counter transmits signals to the comparator whenever the computer system is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

8. The computer system of claim 7, wherein the comparator compares the signal received from the first counter and the data received from the storage register, and wherein the comparator transmits a refresh trigger signal whenever there is a match between the signal and the data.

9. The computer system of claim 4, wherein the refresh timing circuit further comprises a second counter.

10. The computer system of claim 9, wherein the first counter counts the number of clock pulses generated by the clock generator while the computer system is operating in the low power mode and the second counter counts the number of clock pulses generated by the clock generator while the computer system is operating in a normal mode.

11. The computer system of claim 10, wherein the second counter transmits data to the storage register upon the occurrence of a memory refresh event whenever the computer system is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

12. The computer system of claim 11, wherein the second counter is deactivated and the first counter is activated whenever the computer system transitions from the normal mode to the low power mode.

13. The computer system of claim 12, wherein the first counter transmits signals to the comparator whenever the computer system is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

14. The computer system of claim 3, wherein the refresh timing circuit includes a second counter for triggering memory refresh events whenever the computer system is operating in the normal mode

15. The computer system of claim 1, wherein the memory is an Extended Data Out Dynamic Random Access Memory (EDO DRAM) and the memory controller is an EDO DRAM controller.

16. An Extended Data Out Dynamic Random Access Memory (EDO DRAM) controller comprising:

a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

17. The computer system of claim 16, wherein the refresh timing circuit further comprises:

a clock generator;

a first counter coupled to the clock generator;

a storage register coupled to the clock generator and the counter; and

a comparator coupled to the clock generator, the counter and the storage register.

18. The EDO DRAM controller of claim 17, wherein the EDO DRAM controller operates in a normal mode and a low power mode.

19. The EDO DRAM controller of claim 18, wherein the first counter counts the number of clock pulses generated by the clock generator.

20. The EDO DRAM controller of claim 19, wherein the first counter transmits data to the storage register whenever the EDO DRAM controller is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

21. The EDO DRAM controller of claim 20, wherein the storage register transmits the data to the comparator upon a transition from the normal mode to the low power mode.

22. The EDO DRAM controller of claim 21, wherein the first counter transmits signals to the comparator whenever the EDO DRAM controller is operating in the

low power mode, the signal representing the number of clock pulses received from the clock generator.

23. The EDO DRAM controller of claim 22, wherein the comparator compares the signal received from the first counter and the data received from the storage register, and wherein the comparator transmits a refresh trigger signal whenever there is a match between the signal and the data.

24. The EDO DRAM controller of claim 19, wherein the refresh timing circuit further comprises a second counter.

25 . The EDO DRAM controller of claim 24, wherein the first counter counts the number of clock pulses generated by the clock generator while the EDO DRAM controller is operating in the low power mode and the second counter counts the number of clock pulses generated by the clock generator while the EDO DRAM controller is operating in the normal mode.

26. The EDO DRAM controller of claim 25, wherein the second counter transmits data to the storage register upon the occurrence of a memory refresh event whenever the EDO DRAM controller is operating in the normal mode, the data representing the

number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

27. The EDO DRAM controller of claim 26, wherein the second counter is deactivated and the first counter is activated whenever the EDO DRAM controller transitions from the normal mode to the low power mode.

28. The EDO DRAM controller of claim 27, wherein the first counter transmits signals to the comparator whenever the EDO DRAM controller is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

29. A method of calibrating a refresh timer in a computer system, the method comprising:

counting a first set of clock pulses received at a counter from a clock generator;

receiving a signal indicating that a memory refresh event has been triggered; and

storing a first count representing the number of clock cycles received at the counter before receiving the signal.

30. The method of claim 29, further comprising:

resetting the counter after storing the first count;

counting a second set of clock pulses;

receiving the signal indicating that a memory refresh event has been triggered; and

storing a second count.

31. The method of claim 29, wherein the refresh timer is a low power mode refresh timer.

32. In a computer system having a normal mode of operation and a low power mode of operation, a method of triggering a memory refresh event while the computer system is operating in the low power mode, the method comprising:

transmitting a frequency value to a comparator, the frequency value representing the frequency at which to trigger memory refresh events;

transmitting a first clock pulse count to the comparator;

determining whether the first clock pulse count is equal to the frequency value; and

transmitting a first refresh signal.

33. The method of claim 32, further comprising:

transmitting a second clock pulse count to the comparator if it is determined that the first clock pulse is not equal to the frequency value;

determining whether the second clock pulse count is equal to the frequency value; and

transmitting the first refresh signal.

34. The method of claim 32, further comprising transitioning from the normal mode of operation to the low power mode of operation before transmitting the frequency value to the comparator.

35. The method of claim 32, wherein the process of transmitting the first clock pulse count to the comparator further comprises:

transmitting a clock pulse from a clock generator to a counter;

incrementing the counter; and

transmitting the incremented count to the comparator.

36. The method of claim 35, further comprising resetting the counter before transmitting the clock pulse from the clock generator.

37. The method of claim 35, further comprising:

resetting the counter after transmitting the refresh signal;

transmitting a second clock pulse count to the comparator;

determining whether the second clock pulse count is equal to the frequency value; and

transmitting a second refresh signal.

ABSTRACT OF THE DISCLOSURE

According to one embodiment, the present invention discloses a computer system that includes a memory and a memory controller. The memory controller includes a refresh timing circuit that generates clock pulses. The clock pulses are used to trigger memory refresh events. According to a further embodiment, the refresh timing circuit includes a clock generator, a counter coupled to the clock generator and a storage register coupled to the clock generator and counter. Further, the refresh timing circuit includes a comparator coupled to the clock generator, the counter and the storage register.

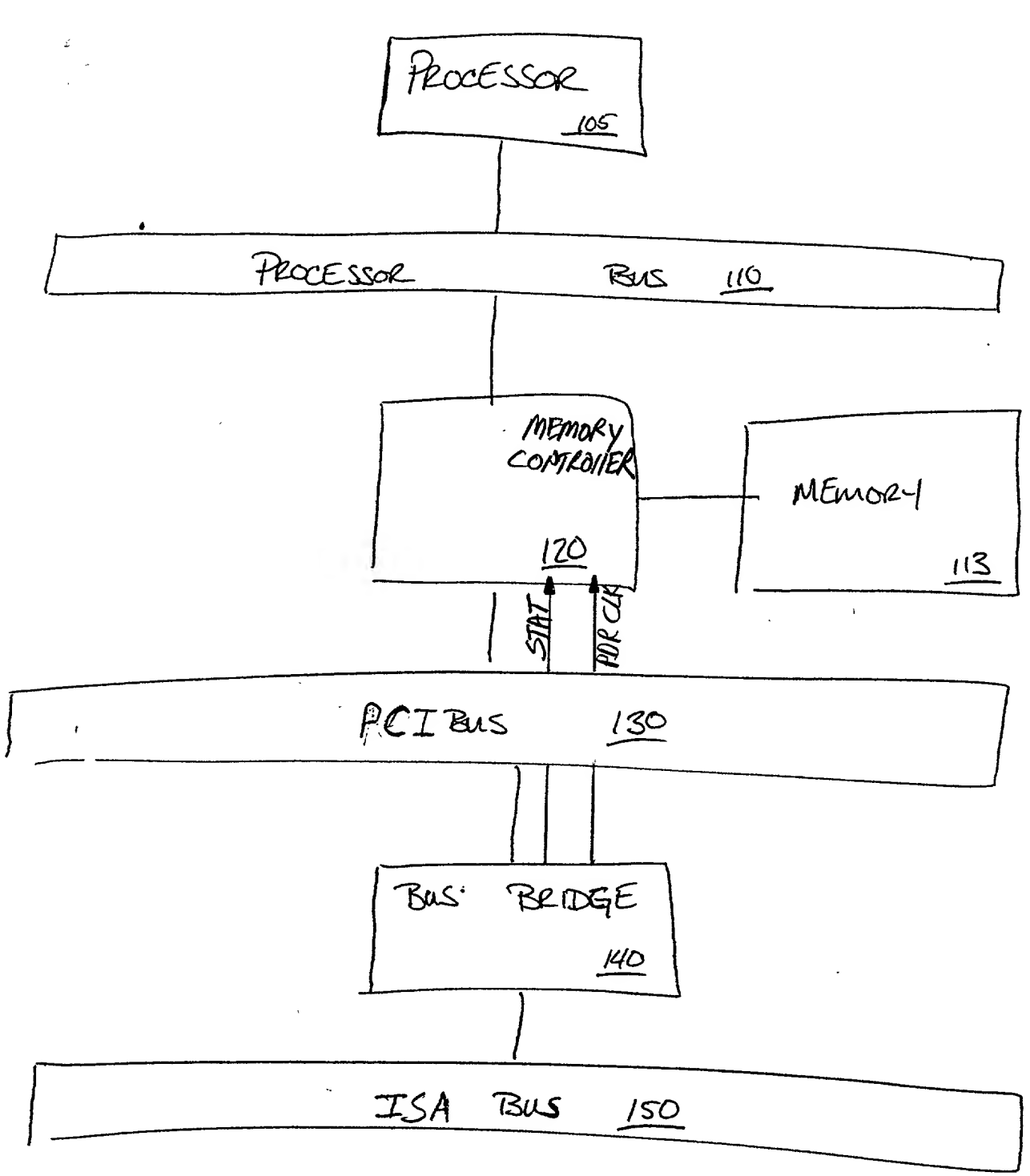


FIG. 1 (PRIOR ART)

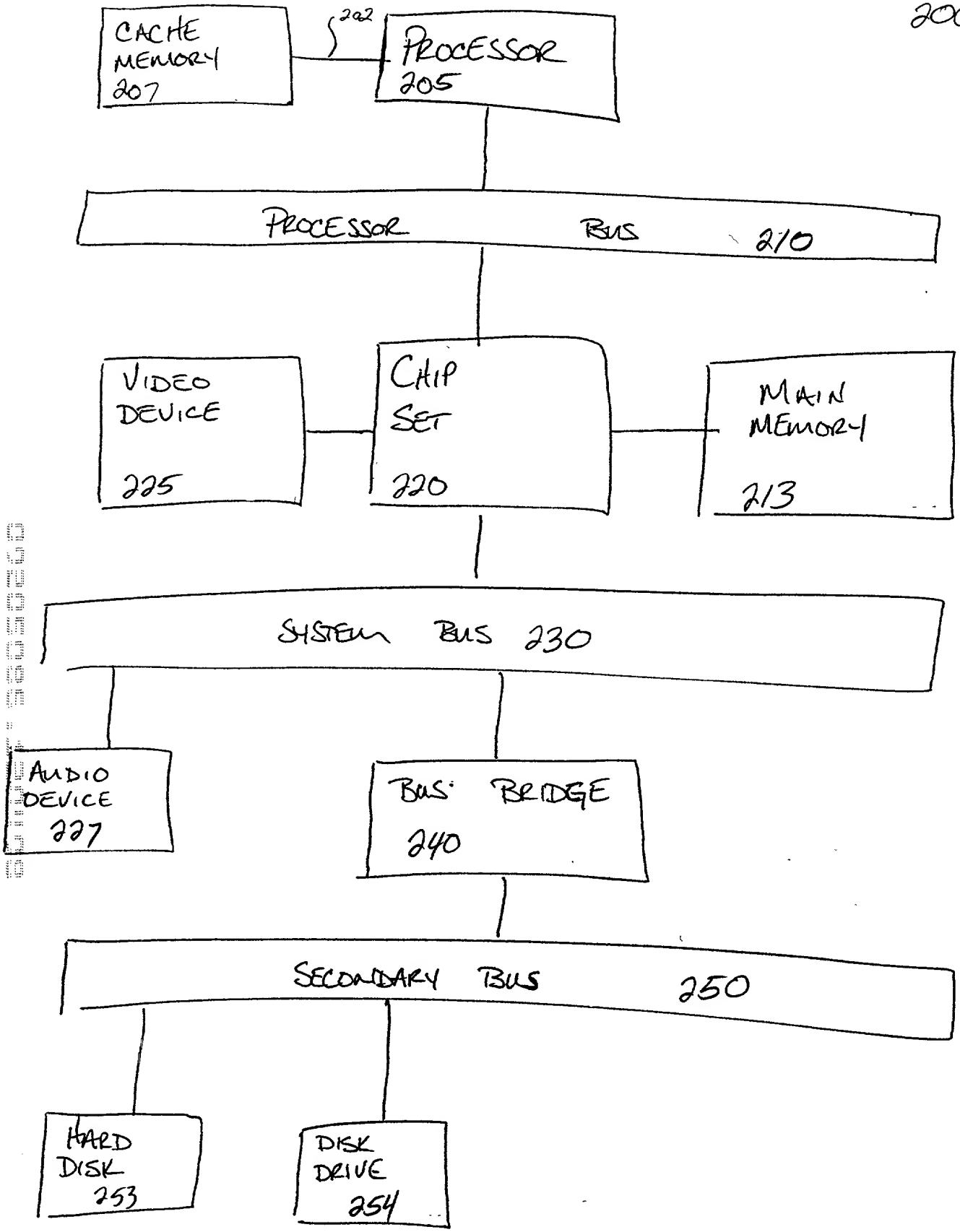

200
CACHE MEMORY 207
202
PROCESSOR 205
PROCESSOR BUS 210
VIDEO DEVICE 225
CHIP SET 220
MAIN MEMORY 213
SYSTEM BUS 230
AUDIO DEVICE 227
BUS BRIDGE 240
SECONDARY BUS 250
HARD DISK 253
DISK DRIVE 254

FIG. 2

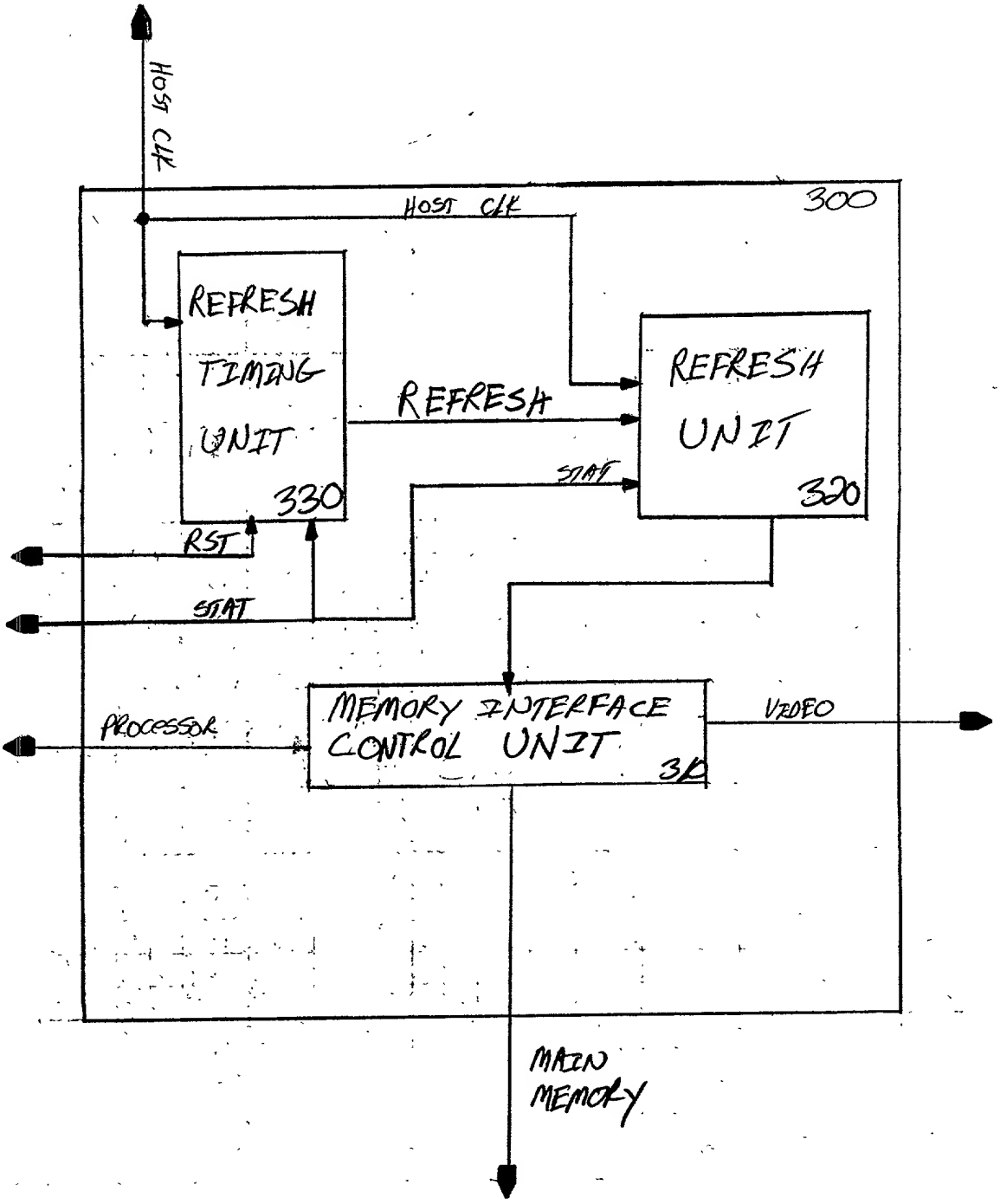
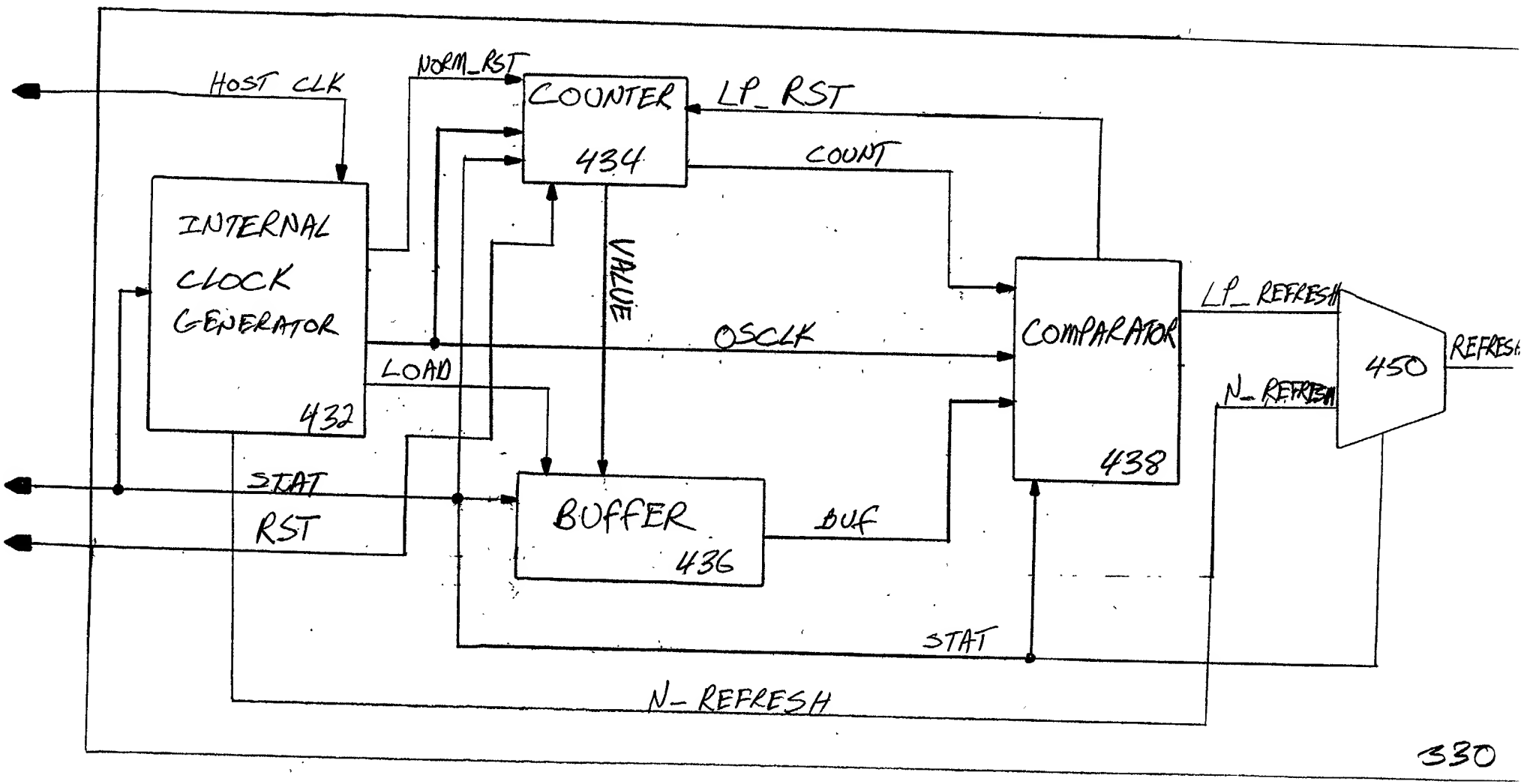


FIG. 3


HOST CLK
NORM_RST
COUNTER
434
LP_RST
COUNT
INTERNAL
CLOCK
GENERATOR
432
VALUE
OSCLK
LOAD
COMPARATOR
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LP_REFRESH
450
N_REFRESH
STAT
RST
BUFFER
436
BUF
STAT
N_REFRESH
330

FIG 4

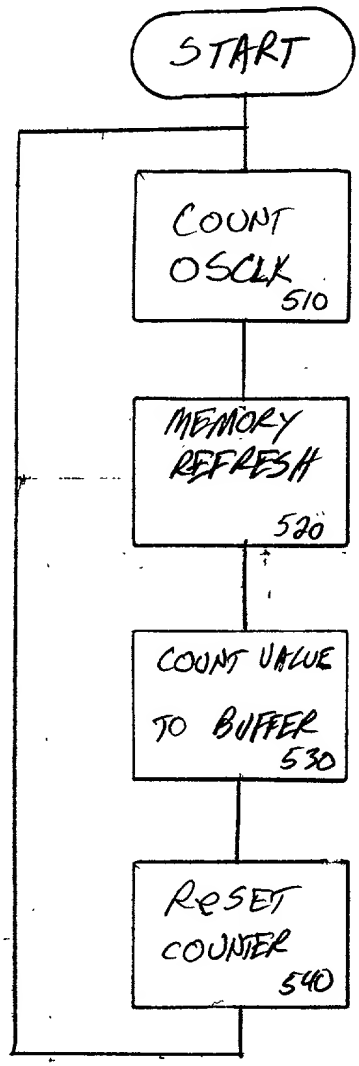


FIG. 5

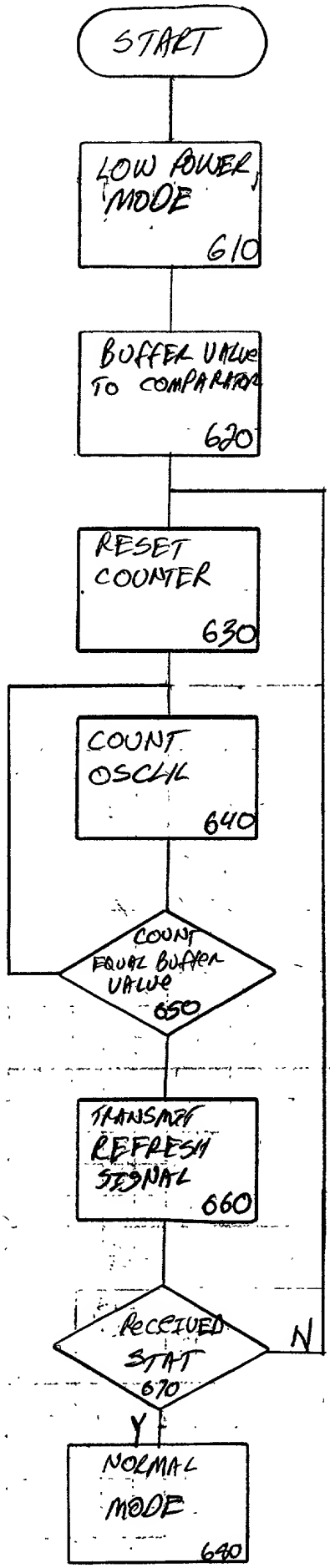
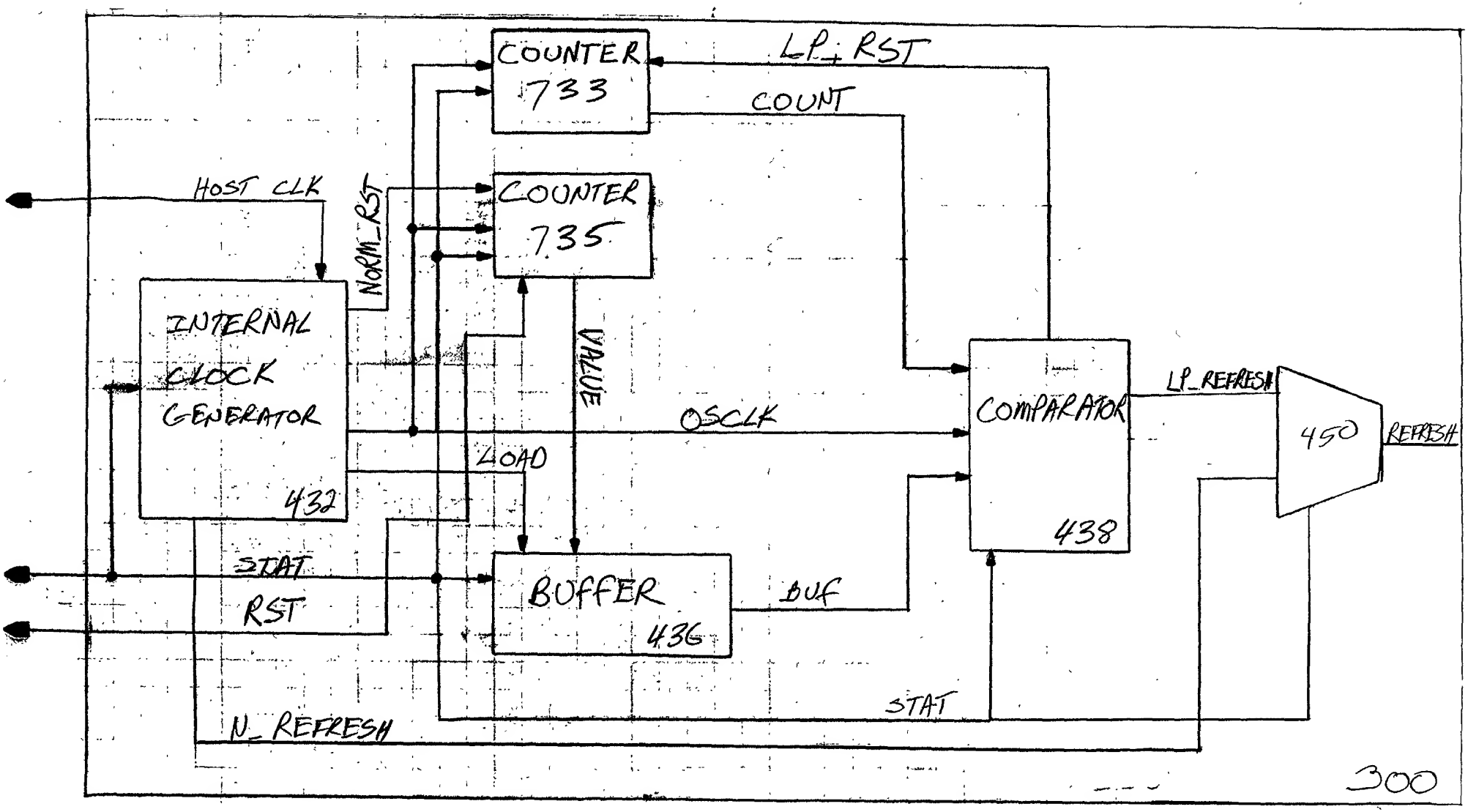


FIG. 6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733
LP_RST
COUNT
HOST CLK
NORM_RST
COUNTER
735
INTERNAL
CLOCK
GENERATOR
432
VALUE
OSCLK
LOAD
COMPARATOR
438
LP_REFRESH
450
REFRESH
STAT
RST
BUFFER
436
BUF
STAT
N_REFRESH
300

FIG. 7

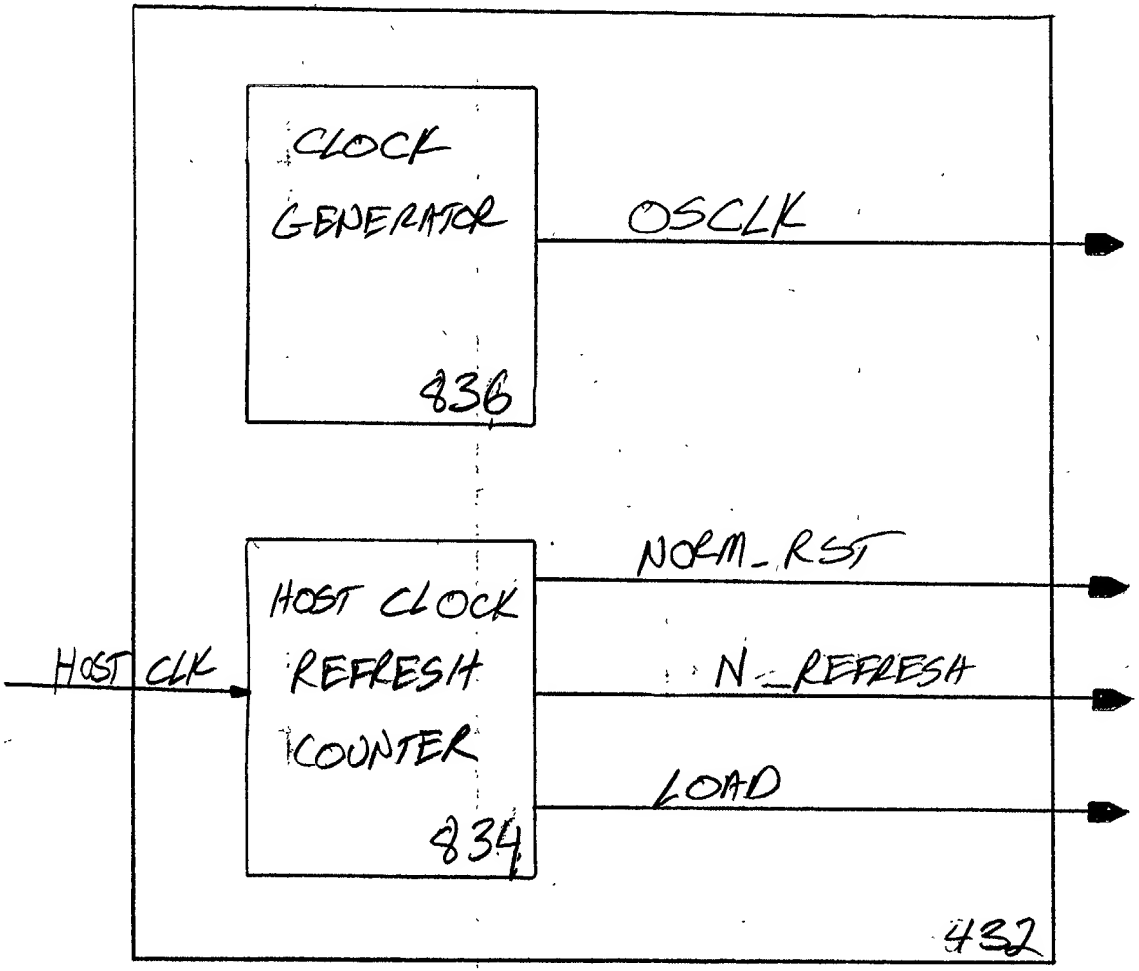

FIG. 8

Attorney's Docket No.: 042390.P5549 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND APPARATUS FOR SELF TIMING REFRESH

the specification of which

___X___ is attached hereto.
_____ was filed on _____ as United States Application Number _____ or PCT International Application Number_____ and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

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(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to Michael J. Mallie, (408) 720-8598.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Full Name of Sole/Third Inventor Vincent Von Bokern
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___ Business Address or other address where mail is customarily received (e.g., P.O. Box).
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(City and State of Residence)

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.